WHAT IS CLAIMED IS:

1. A method of fabricating a ferroelectric memory device comprising the steps of:

forming first and second switching elements on a semiconductor substrate;

forming an interlayer insulating layer covering the first and second switching elements;

forming first and second contact plugs in the interlayer insulating layer, the first and second contact plugs being coupled to the first and second switching elements, respectively;

forming, on the interlayer insulating layer, capacitors where a lower electrode coupled to the first contact plug, a first ferroelectric layer, a middle electrode, a second ferroelectric layer, and an upper electrode are sequentially stacked;

forming an insulating layer covering the capacitor, the second contact plug, and the interlayer insulating layer; and

forming, in the insulating layer, an interconnection for connecting the second contact plug to the upper electrode.

2. The method of Claim 1 further comprising a step of forming a plate line coupled to the middle electrode in the insulating layer.

3. The method of Claim 1, wherein the lower, middle, and the upper electrodes are made of one selected from a group consisting of platinum, iridium oxide, ruthenium oxide, and LaSrCo oxide (LSCO), respectively.

4. The method of Claim 3, wherein the lower electrode is formed of a multi-layer comprising a titanium layer, a titanium nitride layer, an iridium layer, an iridium oxide layer, and a platinum layer sequentially stacked.

5. The method of Claim 1, wherein the ferroelectric layer is made of one selected from a group consisting of lead zirconia titanate (PZT), lead lanthanum zirconia titanate (PLZT), strontium barium titanate (SBT), and barium lanthanum titanate (BLT).

6. A method of fabricating a ferroelectric memory device comprising the steps of:

forming a switching element on a semiconductor substrate;

forming an interlayer insulating layer covering the switching element;

forming a contact plug coupled to the switching element in the interlayer insulating layer;

forming, on the interlayer insulating layer, first and second capacitors comprising a lower electrode, a first ferroelectric layer, a middle electrode, a second ferroelectric layer, and an upper electrode;

forming an insulating layer covering the first and second capacitors, the contact plug, and the interlayer insulating layer; and

forming an interconnection for connecting the contact plug to the middle electrode in the insulating layer.

7. The method of Claim 6 further comprising a step of forming, in the insulating layer, a first plate line coupled to the lower electrode and a second plate line coupled to the upper electrode.

8. The method of Claim 6, wherein the lower, middle, and the upper electrodes are made of one selected from a group consisting of platinum, iridium oxide, ruthenium oxide, and LaSrCo oxide (LSCO), respectively.

9. The method of Claim 8, wherein the lower electrode is formed of a multi-layer comprising a titanium layer, a titanium nitride layer, an iridium layer, an iridium oxide layer, and a platinum layer sequentially stacked.

10. The method of Claim 6, wherein the ferroelectric layer is made of one selected from a group consisting of lead zirconia titanate (PZT), lead lanthanum zirconia titanate (PLZT), strontium barium titanate (SBT), and barium lanthanum titanate (BLT).

11. A method of fabricating a ferroelectric memory device comprising the steps of:

forming a switching element on a semiconductor substrate;

forming an interlayer insulating layer covering the switching element;

forming a contact plug coupled to the switching element in the interlayer insulating layer;

forming, on the interlayer insulating layer, first and second capacitors comprising a lower electrode coupled to the contact plug, a first ferroelectric layer, a middle electrode, a second ferroelectric layer, and an upper electrode sequentially stacked;

forming an insulating layer covering the first and second capacitors and the interlayer insulating layer; and

forming an interconnection for connecting the lower electrode to the upper electrode in the insulating layer.

12. The method of Claim 11 further comprising a step of forming a plate line coupled to the middle layer in the insulating layer.

13. The method of Claim 11, wherein the lower, middle, and the upper electrodes are made of one selected from a group consisting of platinum, iridium oxide, ruthenium oxide, and LaSrCo oxide (LSCO), respectively.

14. The method of Claim 13, wherein the lower electrode is formed of a multi-layer comprising a titanium layer, a titanium nitride layer, an iridium layer, an iridium oxide layer, and a platinum layer sequentially stacked.

15. The method of Claim 11, wherein the ferroelectric layer is made of one selected from a group consisting of lead zirconia titanate (PZT), lead lanthanum zirconia titanate (PLZT), strontium barium titanate (SBT), and barium lanthanum titanate (BLT).